Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants: ALBEROLA et al.

Application No.: 10/743,121

Filing Date: 12/22/2003

For: DIRECT MEMORY ACCESS UNIT WITH INSTRUCTION PRE-DECODER

Confirmation No.: 8465

Group Art Unit: 2183

Examiner: Jacob A. Petranek

RESUBMITTED APPEAL BRIEF

Docket No.: P17377

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Sir:

In accordance with the Notice of Appeal filed May 8, 2007 and the Notice of Non-Compliant Appeal Brief mailed August 6, 2007, Appellants hereby re-submit an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner in the Final Office Action mailed March 8, 2007 (the "Final Office Action") rejecting claims 1, 2, 5-9, 11, 12, 14-17, and 21-24.

REAL PARTY IN INTEREST

The present application is assigned to INTEL CORPORATION, 2200 Mission College Blvd, Santa Clara, CA 95052.

RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known to Applicants or Applicants' legal representative which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal. The present application has not been assigned to any other party.

STATUS OF CLAIMS

Claims 3-4, 10, 13, and 18-20 have been canceled.

Claims 1, 2, 5-9, 11, 12, 14-17, and 21-24 are being appealed.

STATUS OF AMENDMENTS

An Amendment After Final Rejection is filed concurrently herewith to place the application in better condition for the present appeal.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 1

Claim 1 recites that a first instruction can be retrieved from a memory unit and then be pre-decoded at a Direct Memory Access (DMA) unit. For example, FIG. 3 of the present application illustrates a system 300 in which a DMA unit 320 receives and pre-decodes a first instruction from a memory unit 310:

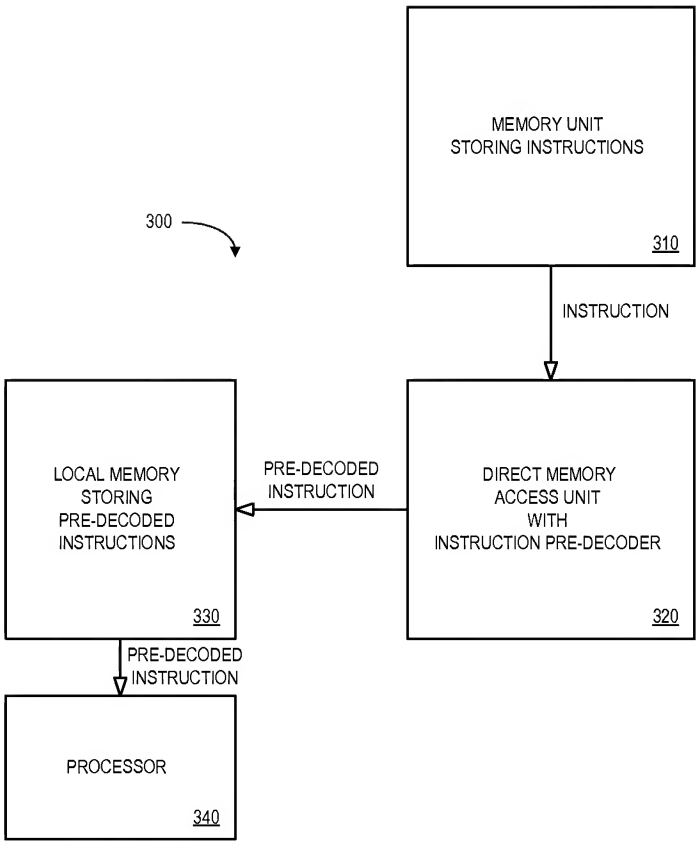

FIG. 3

The DMA unit 320 may then provide the pre-decoded first instruction to a processing element, such as a local memory 330 of a processor 340. Note that the DMA unit 320 might receive the first instruction via an n-bit input path and provide the pre-decoded first instruction via a q-bit output path, where $n < q$. See, *e.g.*, specification at page 5, lines 17-32. That is, the pre-decoded instruction has more bits than the original instruction.

The processor 340 may then completely decode the pre-decoded first instruction and execute that instruction. According to some embodiments, it is determined "that a second instruction subsequent to the first instruction will not be executed." For example, the first instruction might have been a jump instruction, in which case the second instruction would not need to be executed. See, *e.g.*, specification at page 4, lines 1-10. In such cases, it may be arranged "for a pre-decoded second instruction to not be provided from the direct memory access

unit to the processing element." That is, the DMA unit 320 may not need to provide the pre-decoded second instruction to the local memory 330 and/or the processor 340 (since it will not be executed anyway).

Claim 8

Claim 8 is directed to an apparatus including "an n-bit input path to receive a first instruction from a memory unit" and a DMA unit including "an instruction pre-decoder to pre-decode the received first instruction." Moreover, a q-bit output path provides a pre-decoded first instruction from the DMA unit, where $n < q$. See, *e.g.*, specification at page 5, lines 17-32.

Similar to claim 1, a processor is to "(i) receive the pre-decoded first instruction from the q-bit output path, (ii) decode the pre-decoded first instruction, (iii) determine that a second instruction, subsequent to the first instruction, will not be executed, and (iv) arrange for a pre-decoded second instruction not be provided from the direct memory access unit to the processor."

Claim 16

Claim 16 is directed to an article comprising a computer-readable storage medium having stored thereon instructions that when executed by a machine result in performance of a method wherein a first instruction is retrieved from a memory unit via an n-bit input path. For example, FIG. 3 of the present application (reproduced above) illustrates a system 300 in which a DMA unit 320 receives and pre-decodes a first instruction from a memory unit 310.

The DMA unit 320 may then provide the pre-decoded first instruction to a processing element, such as a local memory 330 of a processor 340. Note that the DMA unit 320 might receive the first instruction via an n-bit input path and provide the pre-decoded first instruction via a q-bit output path, where $n < q$. See, *e.g.*, specification at page 5, lines 17-32. That is, the pre-decoded instruction has more bits than the original instruction.

Similarly, second instruction, subsequent to the first instruction may be retrieved from the memory unit and then be pre-decoded at the DMA unit. According to some embodiments, an indication is received from the processing element that the second instruction "will not be

executed." For example, the first instruction might have been a jump instruction, in which case the second instruction would not need to be executed. See, *e.g.*, specification at page 4, lines 1-10. In such cases, the pre-decoded second instruction may be deleted "without providing the pre-decoded second instruction from the direct memory access unit to the processing element." That is, the DMA unit 320 may not need to provide the pre-decoded second instruction to the local memory 330 and/or the processor 340 (since it will not be executed anyway).

Claim 21

Claim 21 is directed to a system including a multi-directional antenna, a processor, and a DMA unit that includes "an n-bit input path to receive a first instruction from a memory unit, an instruction pre-decoder to pre-decode the first instruction, and a q-bit output path to provide a pre-decoded first instruction, where n < q." See, *e.g.*, specification at page 5, lines 17-32. Moreover, as with claim 1, the DMA unit is further "to receive and pre-decode a second instruction without sending the pre-decoded second instruction via the output path."

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 2, 5-9, 11 and 14-17 are rejected under 35 USC 103 as being unpatentable over US Patent No. 6,789,140 ("Kotani") in view of US Patent No. 6,848,041 ("Pechanek").

Claim 12 is rejected under 35 USC 103 as being unpatentable over Kotani in view of Pechanek and further in view of US Patent No. 6,738,836 ("Kessler").

Claim 21 is rejected under 35 USC 103 as being unpatentable over Kotani in view of Pechanek and further in view of US Patent No. 5,265,263 ("Ramsdale").

Claims 22-23 are rejected under 35 USC 103 as being unpatentable over Kotani in view of Pechanek in view of Ramsdale and further in view of US Patent No. 5,291,525 ("Funderbunk").

Claim 24 is rejected under 35 USC 103 as being unpatentable over Kotani in view of Pechanek in view of Ramsdale and further in view of US Patent No. 6,229,796 ("Dent").

ARGUMENTS

Claims 1, 2, 5-9, 11, and 14-17

Claims 1, 2, 5-9, 11 and 14-17 are rejected under 35 USC 103 as being unpatentable over Kotani in view of Pechanek.

FIG. 9 of Kotani discloses a host CPU 210 in communication with a drawing processing unit 230. In particular, the drawing processing unit 230 includes a DMA controller 234 that transfers data from an external main memory 20 to a drawing section 232 within the drawing processing unit 230. As described in Kotani:

> [W]hen preparing data in the main memory 20, the host CPU 210 may insert an interrupt instruction at a position immediately after certain data at which notification of completion of data transfer so far is necessary. The DMA controller 234 predecodes advanced instructions in the drawing data, such as line drawing and filling-in of an area, while transferring the data to the drawing memory 240 or to the drawing section 232. Therefore, when the DMA controller 234 decodes an interrupt instruction, it can generate an interrupt for the host CPU 210 to notify the host CPU 210 of the progress of the transfer.

Col. 11, lines 54-64.

As will now be explained, Appellants respectfully suggest that Kotani fails to disclose or suggest "providing [a] pre-decoded first instruction from the direct memory access unit to a processing element," "decoding the pre-decoded first instruction at the processing element," "executing the completely decoded instruction at the processing element," and "determining, based on said executing, that a second instruction subsequent to the first instruction will not be executed" as recited in claim 1. That is, even if the "line drawing and filling-in of an area" described in Kotani could be considered "pre-decoded instructions," execution of such instructions would not result in a determination that a subsequent instruction will not be executed.

According to the Final Office Action:

> Determining, based on said executing, that a second instruction subsequent to the first instruction will not be executed (Kotani:

> Figure 11 element 239, column 11 lines 20-28)(The drawing end instruction tells that there are no further instructions to execute in the current path. It's obvious to one of ordinary skill in the art that the DMA controller will continually fetch instructions from a current memory area until told to do otherwise. Therefore, the DMA will only be told to do so otherwise at the very earliest when the drawing end instruction is predecoded within the DMA. Since Kotani doesn't disclose the predecoder being used for detecting the drawing end instruction, it's obvious to one of ordinary skill in the art that the drawing end instruction may not be detected until it's fully decoded in the processor. Thus, it would have been obvious to one of ordinary skill in the art that at least one more instruction would have been fetched from memory during the predecoding process, which leaves at least one instruction within the DMA that won't be executed because the drawing has finished processing.)

Final Office Action, last complete paragraph on page 4. Appellants disagree with this logic as it is best understood. In particular, nowhere does Kotani disclose or suggest that a drawing end instruction is predecoded by the DMA controller 234.[1] Thus, Kotani can't been viewed as teaching "providing [a] pre-decoded first instruction from the direct memory access unit to a processing element" (where that instruction will eventually result in a determination that a subsequent instruction will not be executed). Nor can Kotani be viewed as disclosing "decoding the pre-decoded first instruction at the processing element" (that is, there is no teaching or suggestion that a drawing end instruction would be partially decoded by the DMA controller 234 and then completely decoded by the drawing section 232). Finally, Kotani does not disclose or suggest "executing the completely decoded instruction at the processing element" and "determining, based on said executing, that a second instruction subsequent to the first instruction will not be executed" as recited in claim 1.

Moreover, as admitted in the Final Office Action, Kotani completely fails to teach or suggest that the input path of the DMA controller 234 has fewer bits that the output path. Final Office Action, first complete paragraph on page 5.

According to the Final Office Action, Kotani is "silent" on the details of how predecoding works. Final Office Action, last partial paragraph on page 5. Kotani, however, does describe decoding as follows: "The DMA controller 234 predecodes advanced instructions

[1] Instead, Kotani describes that "advanced" instructions, such as line drawing and filling-in of drawing areas, might be predecoded. Col. 11, lines 54-64.

in the drawing data, such as line drawing and filling-in of an area, while transferring the data to the drawing memory 240 or to the drawing section 232." Col. 11, lines 54-64. There is simply no reason why such a process would suggest using more bits in the DMA controller 234 output path as compared to its input path.

Finally, in rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of presenting a *prima facie* case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). A *prima facie* case of obviousness is established by presenting evidence that would have led one of ordinary skill in the art to arrive at the claimed invention.

The teaching or suggestion to make the claimed combination must be found in the prior art, and not based on the Applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). The fact that references can potentially be modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. MPEP 2143.01; Monarch Knitting Machinery Corp. v. Sulzer Morat GmbH, 45 USPQ 2d 1977, 1981-82 (Fed. Cir. 1998) (the question to be asked is "whether the prior art contains a suggestion or motivation to combine references").

According to the Final Office Action, one would have been motivated to modify Kotani in view of the Pechanek as follows:

> One of ordinary skill in the art would have been motivated to find out how predecoding works to find the processor of Pechanek that describes in detail the generation of control signals for instructions to add this functionality. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add the control signal generation aspect of Pechanek for the advantage of realizing how predecoding works.

Final Office Action, first partial paragraph on page 6. Appellants respectfully suggest that this falls far short of a motivation to modify Kotani in specific ways that would result in the

particular invention as recited in claim 1. Appellants also note that the general idea of "pre-decoding" could be done in any number of ways that would not require more bits in the DMA controller 234 output path Kotani as compared to the input path.

The absence of any motivation in the prior art (and the lack of a convincing line of reasoning) to perform the particular method as recited in the pending claims indicates that the Examiner has simply recognized a benefit provided by the present invention, and then used that benefit as a motivation to combine the references – the essence of impermissible hindsight reconstruction.

Because there is no teaching or suggestion to modify the references in this way, a *prima facie* case of obviousness has not been established. The rejection of these claims should be reversed.

Claim 12

Claim 12 is rejected under 35 USC 103 as being unpatentable over Kotani in view of Pechanek and further in view of Kessler. Because claim 12 includes limitations similar to those described above with respect to claim 1, Appellants respectfully request reversal of the rejection for at least the same reasons.

Claim 21

Claim 21 is rejected under 35 USC 103 as being unpatentable over Kotani in view of Pechanek and further in view of Ramsdale. Because claim 21 includes limitations similar to those described above with respect to claim 1, Appellants respectfully request reversal of the rejection for at least the same reasons.

Claims 22-23

Claims 22-23 are rejected under 35 USC 103 as being unpatentable over Kotani in view of Pechanek in view of Ramsdale and further in view of Funderbunk. Because claims 22-23

include limitations similar to those described above with respect to claim 1, Appellants respectfully request reversal of the rejection for at least the same reasons.

Claim 24

Claim 24 is rejected under 35 USC 103 as being unpatentable over Kotani in view of Pechanek in view of Ramsdale and further in view of Dent. Because claim 24 includes limitations similar to those described above with respect to claim 1, Appellants respectfully request reversal of the rejection for at least the same reasons.

CONCLUSION

Appellants respectfully suggest that rejections of claims 1, 2, 5-9, 11, 12, 14-17, and 21-24 are improper and request that the rejections be reversed. If any issues remain, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned.

Respectfully submitted,

August 21, 2007
Date

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Appendix A – Claims

Appendix B – Evidence

Appendix C - Related Proceedings

APPENDIX A - CLAIMS

This is a complete copy of the claims involved in the appeal:

1. A method, comprising:

retrieving a first instruction from a memory unit via an n-bit input path;

pre-decoding the first instruction at a direct memory access unit;

providing the pre-decoded first instruction from the direct memory access unit to a processing element via a q-bit output path, where $n < q$;

decoding the pre-decoded first instruction at the processing element;

executing the completely decoded instruction at the processing element;

determining, based on said executing, that a second instruction subsequent to the first instruction will not be executed; and

arranging for a pre-decoded second instruction to not be provided from the direct memory access unit to the processing element.

2. The method of claim 1, wherein said providing comprises storing the pre-decoded first instruction in memory local to the processing element.

3-4. (Canceled)

5. The method of claim 1, further comprising:

loading instructions into the memory unit during a boot-up process.

6. The method of claim 1, wherein the processing element is a reduced instruction set computer device.

7. The method of claim 6, wherein the pre-decoded first instruction comprises execution control signals.

8. An apparatus, comprising:

an n-bit input path to receive a first instruction from a memory unit;

a direct memory access unit including an instruction pre-decoder to pre-decode the received first instruction;

a q-bit output path to provide a pre-decoded first instruction from the direct memory access unit, where $n < q$; and

a processor to (i) receive the pre-decoded first instruction from the q-bit output path, (ii) decode the pre-decoded first instruction, (iii) determine that a second instruction, subsequent to the first instruction, will not be executed, and (iv) arrange for a pre-decoded second instruction not be provided from the direct memory access unit to the processor.

9. The apparatus of claim 8, further comprising:

the memory unit coupled to the input path.

10. (Canceled)

11. The apparatus of claim 8, wherein the processing element includes a local memory to store the pre-decoded first instruction.

12. The apparatus of claim 8, including a plurality of processing elements, each processing element being associated with a direct memory access unit that includes an instruction pre-decoder.

13. (Canceled)

14. The apparatus of claim 8, wherein the direct memory access unit, the memory unit, and the processing element are formed on an integrated circuit.

15. The apparatus of claim 8, wherein the processing element is a reduced instruction set computer device having an instruction pipeline.

16. An article, comprising:

a computer-readable storage medium having stored thereon instructions that when executed by a machine result in the following:

retrieving a first instruction from a memory unit via an n-bit input path,

pre-decoding the first instruction at a direct memory access unit,

providing via a q-bit output path the pre-decoded first instruction from the direct memory access unit to a processing element to be decoded, where $n < q$,

retrieving a second instruction, subsequent to the first instruction, from the memory unit,

pre-decoding the second instruction at the direct memory access unit,

receiving from the processing element an indication that the second instruction will not be executed, and

deleting the pre-decoded second instruction without providing the pre-decoded second instruction from the direct memory access unit to the processing element.

17. The article of claim 16, wherein said providing comprises storing the pre-decoded first instruction in memory local to the processing element.

18-20. (Canceled)

21. A system, comprising:

a multi-directional antenna;

an apparatus having a direct memory access unit that includes:

an n-bit input path to receive a first instruction from a memory unit,

an instruction pre-decoder to pre-decode the first instruction, and

a q-bit output path to provide a pre-decoded first instruction, where $n < q$, wherein the direct memory access unit is further to receive and pre-decode a second instruction without sending the pre-decoded second instruction via the output path; and

a processor to receive and decode the pre-decoded first instruction received via the q-bit output path.

22. The system of claim 21, wherein the apparatus is a digital base band processor.

23. The system of claim 22, wherein the digital base band processor is formed as a system on a chip.

24. The system of claim 21, wherein the system is a code-division multiple access base station.

APPENDIX B - EVIDENCE

No evidence is submitted herewith (*i.e.*, this appendix is empty).

APPENDIX C - RELATED PROCEEDINGS

No other appeals or interferences are known to Applicants or Applicants' legal representative which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal. The present application has not been assigned to any other party.

Therefore, there are no copies of decisions rendered by a court or the Board to attach (*i.e.*, this appendix is empty).